CS 207 Digital Logic - Spring 2019
Lab 10 - Registers

Monday, Apr. 22, 2019

1 Experiment A

Design and verify a four-bit universal shift register.

2 Experiment B

Design and verify a serial 2's complementer with a shift register and a flip-flop. The binary number is shifted out from one side and it's 2's complement shifted into the other side of the shift register.

Assignment
Save the source code and testbenches in `complementer.v`. Assignment 3 requires the source file.