

CS 207 Digital Logic - Spring 2019

Lab 11 - Registers

Monday, Apr. 29, 2019

1 Experiment A

Design and verify a two-decade BCD counter.

2 Experiment B

Design and verify a four-bit up-down counter with parallel load.

Assignment

Save the source code and testbenches in `up-down.v`. Assignment 3 requires the source file.