CS 207 Digital Logic - Spring 2019
Lab 6 - Combinational Circuit

Monday, Mar. 25, 2019

1 Experiment A

Construct a 16×1 multiplexer with two 8×1 and one 2×1 multiplexers. Design and verify a hierarchical gate-level model of the multiplexer.

2 Experiment B

Design and verify a four-bit adder-subtractor with overflow detection and carry lookahead using gate-level design.

Assignment
Save the source code and testbenches in `addsub.v`. Assignment 2 requires the source file.

3 Experiment C

Design and verify a 3-to-8 decoder using gate-level design. Use the module to implement a 4-to-16 and a 5-to-32 decoder.

Assignment
Save the source code and testbenches in `decoder3.v`, `decoder4.v`, `decoder5.v`, respectively. Assignment 2 requires the source file.