CS 207 Digital Logic - Spring 2019
Lab 7 - Decoder and Encoder

Monday, Apr. 1, 2019

1 Experiment A

1.1 Have a Try

Use the previous 4-to-16 decoder to design and verify a realization of the following logic function: $Y = A'B'C'D' + AB'C' + AB'CD' + ABD + A'B'CD' + BC'D + A'$.

Assignment
Save the source code and testbenches in `logicdec.v`. Assignment 2 requires the source file.

2 Experiment B

2.1 Have a Try

Design a 8-to-1 multiplexer using gate-level design. Use the module to design and verify a realization of the same logic function: $Y = A'B'C'D' + AB'C' + AB'CD' + ABD + A'B'CD' + BC'D + A'$.

Assignment
Save the source code and testbenches in `logicmux.v`. Assignment 2 requires the source file.