CS 207 Digital Logic - Spring 2019
Lab 8 - Latches and Flip-flops

Monday, Apr. 8, 2019

1 Experiment A

Design and verify a gate-level positive-edge-sensitive D flip-flop.

2 Experiment B

Design and verify D, JK, and T flipflops with behavioral modelling.

Assignment
Save the source code and testbenches in `flipflops.v`. Assignment 2 requires the source file.

3 Experiment C

Design and verify a JK flipflop with set and reset control in UDP.

Assignment
Save the source code and testbenches in `jkff.v`. Assignment 2 requires the source file.